	Document ID	Issue Date	Pages	Title	Current OR
1	US 20030112915 A1	20030619	17	Lock detector circuit for dejitter phase lock loop (PLL)	375/376
2	US 6778623 B1	20040817	11	Apparatus for synchronizing the frame clock in units/nodes of data-transmitting systems	375/376
3	US 6765445 B2	20040720	35	Digitally-synthesized loop filter circuit particularly useful for a phase locked loop	331/17
4	US 6731667 B1	20040504	25	Zero-delay buffer circuit for a spread spectrum clock system and method therefor	375/130
5	US 6630868 B2	20031007	35	Digitally-synthesized loop filter circuit particularly useful for a phase locked loop	331/17
6	US 6614317 B2	20030902	9	Variable lock window for a phase locked loop	331/17
7	US 6356129 B1	20020312	24	Low jitter phase-locked loop with duty-cycle control	327/175
8	US 6289069 B1	20010911	6	Digital filter for rotation correction loop of a QPSK or QAM demodulator	375/376
9	US 5889828 A	19990330	103	Clock reproduction circuit and elements used in the same	375/374
10	US 5757652 A	19980526	13	Electrical signal jitter and wander measurement system and method	702/69

	Current XRef	Inventor
1		Meltzer, David
2	327/147; 327/156	Dietrich; Werner et al.
3	331/11; 331/16; 331/18; 331/25; 375/247; 375/376	Perrott; Michael H. et al.
4	375/373; 375/375; 375/376	Lee; Kyeongho et al.
5	331/1A; 331/158; 331/177R; 375/373; 375/376	Perrott; Michael H. et al.
6	327/156; 331/1A; 331/DIG.2 ; 375/376	Wong; Keng L. et al.
7	327/156; 327/294; 375/376	O'Brien; David E. et al.
8	327/156; 375/327	Meyer; Jacques
9	327/154; 375/375; 375/376	Miyashita; Takumi et al.
10	375/371; 375/376	Blazo; Stephen F. et al.

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11	US 5754437 A	19980519	24	Phase measurement apparatus and method	702/75
12	US 5610954 A	19970311	103	Clock reproduction circuit and elements used in the same	375/375
13	US 5337335 A	19940809	10	Phase locked loop with frequency deviation detector and decoder circuit comprising such a phase locked loop	375/376
14	US 5012494 A	19910430	15	Method and apparatus for clock recovery and data retiming for random NRZ data	375/376
15	US 4870660 A	19890926	10	Variable frequency rate receiver	375/327
16	US 4590602 A	19860520	9	Wide range clock recovery circuit	375/375

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11	327/156; 327/159; 370/516; 375/226; 375/371; 375/373; 375/375; 375/376; 702/69; 702/79; 708/313	Blazo; Stephen F.
12	327/157; 331/25; 375/374	Miyashita; Takumi et al.
13	327/156; 331/17; 331/32; 331/34	Cloetens; Henri et al.
14	331/17	Lai; Benny W. H. et al.
15	331/14; 375/329; 375/376	Keate; Christopher R.
16	331/1A; 331/DIG.2; 375/328; 375/374; 375/376	Wolaver; Dan H.

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1	US 20040101080 A1	20040527	16	Sigma-delta modulator and fractional-N frequency synthesizer comprising same	375/375
2	US 20040008804 A1	20040115	10	Method and device for controlling stuffing	375/375
3	US 20030053576 A1	20030320	27	Linear phase detector for high-speed clock and data recovery	375/375
4	US 6792064 B2	20040914	28	Multiple phase-locked loop circuit	375/376
5	US 6735181 B1	20040511	8	Wireless transceiver with subtractive filter compensating both transmit and receive artifacts	370/290
6	US 6731667 B1	20040504	25	Zero-delay buffer circuit for a spread spectrum clock system and method therefor	375/130
7	US 6674824 B1	20040106	18	Method and circuitry for controlling a phase-locked loop by analog and digital signals	375/376

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1		Lee, Kun-Seok
2		Honken, Stefan et al.
3	375/376	Cao, Jun
4	327/148; 327/157; 331/DIG.2; 375/374; 375/375	Nakamura; Satoshi
5	375/219; 375/375; 375/376; 455/24	Babitch; Daniel
6	375/373; 375/375; 375/376	Lee; Kyeongho et al.
7	375/373; 375/374; 375/375	Chiueh; Tzi-Dar et al.

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8	US 6636575 B1	20031021	14	Cascading PLL units for achieving rapid synchronization between digital communications systems	375/376
9	US 6577695 B1	20030610	10	Emulating narrow band phase-locked loop behavior on a wide band phase-locked loop	375/375
10	US 6526111 B1	20030225	10	Method and apparatus for phase locked loop having reduced jitter and/or frequency biasing	375/376
11	US 6317161 B1	20011113	14	Horizontal phase-locked loop for video decoder	348/536
12	US 5939947 A	19990817	11	Phase synchronous circuit	331/11

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8	327/149; 327/150; 331/17; 341/126; 341/128; 341/129; 341/143; 341/144; 341/146; 341/61; 375/241; 375/242; 375/282; 375/354; 375/371; 375/373; 375/374; 375/375; 375/377	Ott; Stefan
9	327/145; 327/147; 327/156; 327/163; 331/25; 375/376	Everitt; James et al.
10	327/157; 375/374; 375/375	Prasad; Ammisetti V
11	327/147; 348/537; 375/375; 375/376	Renner; Karl et al.
12	327/159; 327/160; 331/1A; 331/14; 331/25; 375/375	Nakao; Takehiko et al.

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13	US 5889828 A	19990330	103	Clock reproduction circuit and elements used in the same	375/374
14	US 5764709 A	19980609	25	Jitter attenuator	375/375
15	US 5754437 A	19980519	24	Phase measurement apparatus and method	702/75
16	US 5651035 A	19970722	8	Apparatus for reducing jitter of a spectrum spread clock signal and method therefor	375/373
17	US 5644605 A	19970701	25	Jitter attenuator	375/375
18	US 5638140 A	19970610	11	FPLL having AFC filter with limited phase shift	348/735
19	US 5610954 A	19970311	103	Clock reproduction circuit and elements used in the same	375/375

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13	327/154; 375/375; 375/376	Miyashita; Takumi et al.
14	327/12; 327/236; 331/11; 375/371	Whiteside; Frank A.
15	327/156; 327/159; 370/516; 375/226; 375/371; 375/373; 375/375; 375/376; 702/69; 702/79; 708/313	Blazo; Stephen F.
16	327/156; 375/375	Tozun; Orhan et al.
17	327/12; 375/371	Whiteside; Frank A.
18	331/34; 348/727; 375/326; 375/344; 375/374; 375/375; 455/192.2	Krishnamurthy; Gopalan et al.
19	327/157; 331/25; 375/374	Miyashita; Takumi et al.

	Document ID	Issue Date	Pages	Title	Current OR
20	US 5592515 A	19970107	28	Fully digital data separator and frequency multiplier	375/340
21	US 5553100 A	19960903	29	Fully digital data separator and frequency multiplier	375/340
22	US 5276716 A	19940104	17	Bi-phase decoder phase-lock loop in CMOS	375/376
23	US 4590602 A	19860520	9	Wide range clock recovery circuit	375/375

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20	327/156; 327/160; 327/166; 375/359; 375/360; 375/371; 375/373; 375/375; 375/376	Saban; Rami et al.
21	327/156; 327/160; 327/166; 375/359; 375/360; 375/371; 375/373; 375/375; 375/376	Saban; Rami et al.
22	331/1A; 375/374; 375/375	Wincn; John M.
23	331/1A; 331/DIG.2; 375/328; 375/374; 375/376	Wolaver; Dan H.